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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/067,721	04/28/1998	TAKURO YAMAMOTO	P/3156-3	1544

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EXAMINER

SRIVASTAVA, VIVEK

ART UNIT

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17

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 09/067,721	Applicant(s) YAMAMOTO, TAKURO	
	Examiner Vivek Srivastava	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 October 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12, 14 and 15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 18) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 U.S.C. § 103

I. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

II. Claims 1, 2, and 4 - 8, are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959) and in view of Huang et al (5,682,522).

Regarding claim 1, Applicant's background discloses a video data transfer system (page 1 lines 8 - 10), a real time output path (page 1 lines 22 - 25, fig 3 item 25) through which video data processed by a video processor (fig 3 item 21) is sent to a display (fig 3 item 16) via a frame buffer (fig 3 item 14), a capturing path (page 2 lines 1 - 6 21 - 38, fig 3 item 27) which is independent of real time output path (fig 3 - capture-only path 27 to FIFO memory 24 and system memory 18 via system bus 17 is separate from real time output path 25 to display 16 via display control circuit 22) and through which video data is sent to a system memory via a system bus (page 2 lines 1- 6, fig 3 items 17 and 18).

The conventional video data transfer system in Applicant's background fails to disclose a capturing path which sends data to a system memory and not through the

frame buffer. Huang depicts transferring data from a CPU to display via frame buffer over paths A, B, and C and transferring data from a CPU to system memory via separate paths G, F, E and D (see fig 3). It would have been obvious modifying Applicant's background to include the claimed capturing path which sends data to a system memory and not through the frame buffer would have enabled separate paths which would reduced congestion in transferring data which would also result in faster data transfer. Therefore, it would have been obvious to one skilled in the art to modify Applicant's background to include the claimed limitation to reduce congestion and increase system speed.

The conventional video data transfer system in Applicant's background fails to disclose the claimed gate in the capturing path. A patent issued to George teaches a television receiver comprising two terminals and a gate wherein the gate can be enabled or disabled thereby permitting or preventing signal flow between the terminals (see col 2 lines 46 - 57). It would have been obvious modifying the conventional video transfer system in Applicant's background to include a controllable gate enabling passing or blocking of video data would have prevented the passing of unwanted video data between the video processor and system memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the conventional video transfer system in Applicant's background to include the claimed gate to ensure the passing of data between the video processor and system memory only when required.

Considering claim 2, the conventional video transfer system in Applicant's background discloses a real time output path (fig 3 items 21, 14, 25, 16, page 1 lines 19 - 24), a capturing path which is independent of the real time output path (fig 3 items 27, 17, 18, page 2 lines 1- 6, capturing only path 27 is independent from realtime output

path 25), a real time output path comprising an offscreen memory which receives video data from video processor via a data bus and stored video data therein, the offscreen memory being in the frame buffer (fig 3 items 25, 14, 21, 13, 15 page 1 lines 19 - 24), a display control circuit which receives video data from the off-screen memory via the data bus for enlargement and interpolation processing and transfers results to the display (page 1 lines 8 - 24, fig 3 items 22, 13, 25, 16), and a capturing path which comprises a memory means for storing video data for transferring the video data to the system bus (page 2 lines 1 - 6, fig 3 items 24, 17, and 18).

The conventional video data transfer system in Applicant's background fails to disclose a capturing path which sends data to a system memory and not through the frame buffer. Huang depicts transferring data from a CPU to display via frame buffer over paths A, B, and C and transferring data from a CPU to system memory via separate paths G, F, E and D (see fig 3). It would have been obvious modifying Applicant's background to include the claimed capturing path which sends data to a system memory and not through the frame buffer would have enabled separate paths which would reduced congestion in transferring data which would also result in faster data transfer. Therefore, it would have been obvious to one skilled in the art to modify Applicant's background to include the claimed limitation to reduce congestion and increase system speed.

The conventional video data transfer system in Applicant's background fails to disclose the claimed gate in the capturing path. A patent issued to George teaches a television receiver comprising two terminals and a gate wherein the gate can be enabled or disabled thereby permitting or preventing signal flow between the terminals (see col 2 lines 46 - 57). It would have been obvious modifying the conventional video transfer system in Applicant's background to include a controllable gate enabling

passing or blocking of video data would have prevented the passing of unwanted video data between the video processor and system memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the conventional video transfer system in Applicant's background to include the claimed gate to ensure the passing of data between the video processor and system memory only when required.

Considering claim 4, the conventional video transfer system in Applicant's background discloses a capture path memory in a capture path (fig 3 item 24). The Applicant's background fails to disclose a capture path memory being connected to a gate and capture path memory being operable to store the video data passed by the gate. As discussed in claim 1, it would have been obvious to include a gate to ensure passing of data between the video processor and system only when required thus preventing unwanted data from reaching the system memory. It would have been obvious connecting the gate as claimed would have ensured passing data to the system memory only when required thus preventing unwanted data from being stored in the capture path memory.

Considering claim 5, the conventional video transfer system in Applicant's background discloses wherein capture path memory is further effective to transfer the video data to system bus (page 2 lines 1 - 5, fig 3 item 24 and 17).

Considering claim 6, the conventional video transfer system in Applicant's background discloses wherein real time output path comprises an off-screen memory effective to receive video data from the video processor via a data bus and store video data therein (fig 3 - off-screen memory 15 receives video data from video processor 21 via a data bus 13) and offscreen memory is in frame buffer (fig 3 items 14 and 15).

Considering claim 7, the conventional video transfer system in Applicant's background discloses providing video data from video processor to a plurality of paths independent of each other (fig 3 data from video processor is provided to frame buffer data bus path 13 and capture path 27 and real time output path 25), sending video data to a display through a frame buffer in at least one of independent paths operating as a real time output path (fig 3 - data is sent through frame buffer 14 to display 16 via independent real time output path 25, page 1 lines 19 - 24), sending video data to a system memory through a system bus in at least another of independent paths operating as a capture path (fig 3 items 27, 24, 17 and 18, page 2 lines 1 - 6).

The conventional video data transfer system in Applicant's background fails to disclose a capturing only path which sends data to a system memory and not through the frame buffer. Huang depicts transferring data from a CPU to display via frame buffer over paths A, B, and C and transferring data from a CPU to system memory via separate paths G, F, E and D (see fig 3). It would have been obvious modifying Applicant's background to include the claimed capturing path which sends data to a system memory and not through the frame buffer would have enabled separate paths which would reduced congestion in transferring data which would also result in faster data transfer. Therefore, it would have been obvious to one skilled in the art to modify Applicant's background to include the claimed limitation to reduce congestion and increase system speed.

The conventional video transfer system in Applicant's background fails to disclose controlling capture path to permit video data to pass to system memory when video data is to be captured. A patent issued to George teaches a television receiver comprising two terminals and a gate wherein the gate can be enabled or disabled thereby permitting or preventing signal flow between the terminals (see col 2 lines 46 -

57). It would have been obvious modifying the conventional video transfer system in Applicant's background to include a controllable gate would have enabled controlling the capture path for passing or blocking of video data between the video processor and system memory. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the conventional video transfer system in Applicant's background to include the claimed controlling the capture path to ensure the passing of data between the video processor and system memory only when required.

Considering claim 8, the conventional video transfer system in Applicant's background discloses storing video data in a capture path memory in capture path when video data is permitted to pass to system memory (page 2 lines 1 - 6 and fig 3 items 24, 17, and 18, if data is passed to memory 18 it must first be saved in FIFO 24).

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of Huang.

Regarding claim 14, Applicant's background discloses directing and storing data in system memory 18 which inherently meets the claimed "determining whether the video data is to be capture" (see fig 3), processing the video data (met by video processor 21 in fig 3), forwarding the processed video data to a first path, the first path including a display control circuit (22) and a frame buffer (14); note: first path met by path 25. Further, the Applicants disclose forwarding the processed video data to a second path when the determining indicates that the video data is to be captured (this feature is inherent in the figure 3 of the applicant's background since a determination

must be made to route the data to capture path 27-second path or realtime output path 25-first path.

Applicant's background fails to disclose the claimed second path not including the frame buffer. Huang depicts transferring data from a CPU to display via frame buffer over paths A, B, and C and transferring data from a CPU to system memory via separate paths G, F, E and D (see fig 3). It would have been obvious modifying Applicant's background to include the claimed second path which sends data to a system memory and not through the frame buffer would have enabled separate paths which would reduced congestion in transferring data which would also result in faster data transfer. Therefore, it would have been obvious to one skilled in the art to modify Applicant's background to include the claimed limitation to reduce congestion and increase system speed.

Considering claim 15, Applicant's background discloses a video processor 21 which receives video data and processes the video data (see fig 3), a display path 25 coupled to video processor 21, the display path including a frame buffer 14 (see fig 3), the display path conveys the processed video data from the video processor to a display (16). Applicant's background further discloses a capturing path 27 coupled to the video processor, the capturing path 27 conveys the processed data from the video processor 21 to a system memory 18.

The Applicant's background fails to disclose the claimed capturing path not including the frame buffer. Huang depicts transferring data from a CPU to display via frame buffer over paths A, B, and C and transferring data from a CPU to system memory via separate paths G, F, E and D (see fig 3). It would have been obvious modifying Applicant's background to include the claimed capturing path which sends data to a system memory and not through the frame buffer would have enabled

separate paths which would reduced congestion in transferring data which would also result in faster data transfer. Therefore, it would have been obvious to one skilled in the art to modify Applicant's background to include the claimed limitation to reduce congestion and increase system speed.

III. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959), as applied to claim 2 above, and further in view of Przybyla et al (5,982,781) and Soo (5,570,306).

Considering claim 3, the combination of the Applicant's background and George fails to disclose wherein the memory means transfers stored video data to the system bus when system bus is not occupied by some other unit and when system bus is occupied by some other unit, checks if stored data contains a field delimiter or a frame delimiter and closes said gate to stop data transfer when stored data contains the delimiter and, when the stored data does not contain the delimiter, stores the next video data passing through the gate.

Przybyla teaches by checking if a bus is occupied or not before data transmission, loss of data and re-transmission of data is avoided. It would have been obvious to modify the combination of the Applicant's background and George to check to see if the system bus is occupied by other devices to prevent loss of data or re-transmission of data. Soo teaches a frame delimiter can be used to indicate a buffer overflow condition (col 11 lines 1- 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of the Applicant's background and George based on the teachings of Przybyla and Soo to include checking of the system bus as claimed and to include

checking the video data stored in the capture path memory for a frame delimiter to ensure data is not lost or would need re-transmission and to prevent an overflow condition in the capture path memory.

IV. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959), as applied to claim 8 above, and further in view of Przybyla et al (5,982,781).

Considering claim 9, the Applicant's background and George fail to disclose checking system bus for occupation by other devices connected thereto.

Przybyla teaches by checking if a bus is occupied or not before data transmission, loss of data and re-transmission of data is avoided. It would have been obvious to modify the combination of the Applicant's background and George to check to see if the system bus is occupied by other devices to prevent loss of data or re-transmission of data. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of the Applicant's background and George based on the teachings of Przybyla to include checking of the system bus as claimed to ensure data is not lost or would need re-transmission.

Regarding claim 10, the combination of Applicant's background and George fails to disclose the claimed transferring video data from capture path memory to system memory when system bus is not occupied by other devices connected thereto.

It would have been obvious from the teaches of Przybyla, as discussed in claim 9, checking to see if the system bus is not occupied by another device before transferring data would have avoided data loss and the need for re-transmitting data.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of Applicant's background and George to include transferring video data from capture path memory to system memory when system bus is not occupied by other devices connected thereto to avoid data loss and the need for re-transmission.

V. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's background in view of George (3,980,959), and further in view of Przybyla et al (5,982,781) as applied to claim 10 above, and further in view of Soo (5,570,306).

Regarding claim 11, the combination of Applicant's background, George and Przybyla fail to disclose checking video data stored in the capture path memory for at least one of a field and a frame delimiter when the system bus is occupied. Soo teaches a frame delimiter can be used to indicate a buffer overflow condition (col 11 lines 1 - 10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combination of the Applicant's background, George and Przybyla to include checking the video data stored in the capture path memory for a frame delimiter to prevent an overflow condition in the capture path memory.

Regarding claim 12, the combination of the Applicant's background, George and Przybyla fail to disclose controlling capture path to prevent video data from being stored in the capture path memory when the capture path memory contains a frame delimiter.

As discussed in claim 11, from the teachings of Przybyla, it would have been obvious to include checking for a frame delimiter to prevent an overflow condition in the

capture path memory. It would have been obvious to control the capture path to prevent video data from being stored in the capture path memory when the capture path memory contains a frame delimiter to prevent further overflow of the capture path memory.

Response to Arguments

Applicant argues that the combination of the art fails to show or suggest the claimed "a capturing path which is independent of said real time output path and through which said video data is sent to a system memory via a system bus and not through the frame buffer.

The Examiner directs Applicants to rejection above as the combined references disclose the claimed limitation.

Applicant argues that the combination of references fails to disclose limitations in claim 7, in particular, sending said video data to a system memory through a system bus and not through the frame buffer in at least another of said independent paths operating as a capture path.

The Examiner directs Applicants to rejection above as the combined references disclose the claimed limitation.

Applicant argues that the combination of references fails to disclose forwarding the processed video data to a first path, the first path including a display control circuit and a frame buffer, and forwarding the processed video data to a second path when the determining indicates that the video data is to be captured, the second path not including the frame buffer.

The Examiner directs Applicant to rejection above as the combined references disclose the claimed limitation.

As per request, the Examiner has provided a detailed rejection of claims 13 and 14.

Conclusion

VI. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Reddy (6,081,279) - Shared memory graphics accelerator system

Storm et al (5,999,196) - Processing units for graphics accelerator

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

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or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308- 5359 (for informal or draft communications, please label
"PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121

Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vivek Srivastava whose telephone number is (703) 305


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- 4038. The examiner can normally be reached on Monday - Thursday from 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andy Faile, can be reached at (703) 305 - 4380.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 305 - 3900.

12/14/02
VS



VIVEK SRIVASTAVA
PATENT EXAMINER